WHAT IS CLAIMED IS:

1. An integrated circuit having a multiprocessor architecture, the circuit comprising:

a first processor, which operates synchronously with a first internal clock signal;

a second processor, which operates synchronously with a second internal clock signal;

a memory, which operates synchronously with a third internal clock signal; and

a clock supply unit, which generates, from an external clock signal, three clock signals that are in phase with each other, and which supplies the clock signals as the first, second and third internal clock signals, respectively;

wherein the first processor, the second processor, the memory, and the clock supply unit are integrated together on a single chip.

2. The integrated circuit of Claim 1, wherein the memory comprises:

a memory array which is used to store data, and

a memory controller interposed between the first processor and the memory array and between the second processor and the memory array,

wherein the memory controller,

receives a first memory access signal, a first address, a

second memory access signal and a second address, the first memory access signal and the first address being output by the first processor, the second memory access signal and the second address being output by the second processor;

selects and provides the first address to the memory array when the first memory access signal is asserted; and

selects and provides the second address to the memory array when the second memory access signal is asserted.

3. The integrated circuit of Claim 1, wherein the clock supply unit further,

receives a first terminating signal and a second terminating signal;

stops supplying all of the first, second and third internal clock signals when the first and second terminating signals are asserted at the same time;

stops supplying only the first internal clock signal when the first terminating signal is solely asserted; and

stops supplying only the second internal clock signal when the second terminating signal is solely asserted.

4. The integrated circuit of Claim 1 further comprising a reset control unit that is integrated on the chip, the reset control unit supplying a first internal reset signal, a second internal reset signal and a third internal reset sig-

nal, the first internal reset signal being used for resetting the memory, the second internal reset signal being used for resetting the first processor, the third internal reset signal being used for resetting the second processor,

wherein the reset control unit,

receives a first external reset signal, a second external reset signal, and a third external reset signal;

asserts all of the first, second and third internal reset signals when the first external reset signal is asserted;

asserts only the second internal reset signal when the second external reset signal is asserted; and

asserts only the third internal reset signal when the third external reset signal is asserted.

5. The integrated circuit of Claim 4, wherein the clock supply unit further,

receives a first terminating signal and a second terminating signal;

stops supplying all of the first, second and third internal clock signals when the first and second terminating signals are asserted at the same time;

stops supplying only the first internal clock signal when the first terminating signal is solely asserted; and

stops supplying only the second internal clock signal when the second terminating signal is solely asserted.